ADH-Tech

HF302GD Module Datasheet

We are dedicated to developing sensing technology, and providing customers with an innovative and diverse range of sensor products.

Our sensors and state-of-the-art fingerprint recognition algorithm technologies provide advanced and convenient fingerprint acquisition and verification.

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Table of Contents

1. Features

- **Complete Fingerprint Sensor Module:**
  - HF302GT Sensor with iG102CL Sensor Controller
  - Module Size: 35mm x 23mm x 5mm
  - Connector used: BL123H-10R-TAND (10 pin/pitch 1.0mm)
  - Housing Material: Steel
  - ESD Tolerance: +/- 15KV
  - FPS: 9.3/sec
- **HF302GT Sensor:**
  - Pixel: 256 x 360
  - Pixel Size: 50 um x 50 um
  - Spatial Resolution: 508 dpi
  - Sensing Area: 12.8mm x 18mm
- **iG102CL Controller**
  - SPI Clock: 16MHz
  - Package: LGA 84 pin
  - Package Size: 7mm x 7mm x 0.8mm
- **Power Consumption:**
  - Total Supply Current: 15 mA
  - Standby Current: 60 uA
  - Sleep Current: 37 uA
- **Environmental Specification**
  - Operating temperature: -20° C to +70° C
  - Storage temperature: -40° C to +85° C
  - RoHS compliant and low-halogen
  - RCA: 200 cycle
  - Pencil Hardness: 7H
  - Cross cut: 5B
  - PIV Certification

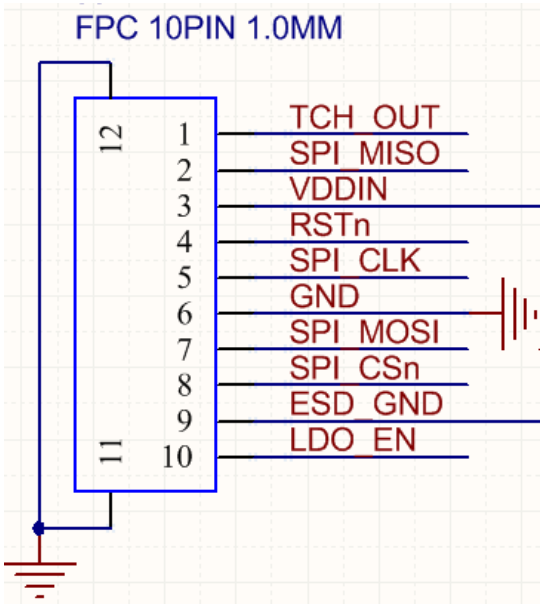
2. Module Structure

Bottom View

Top View

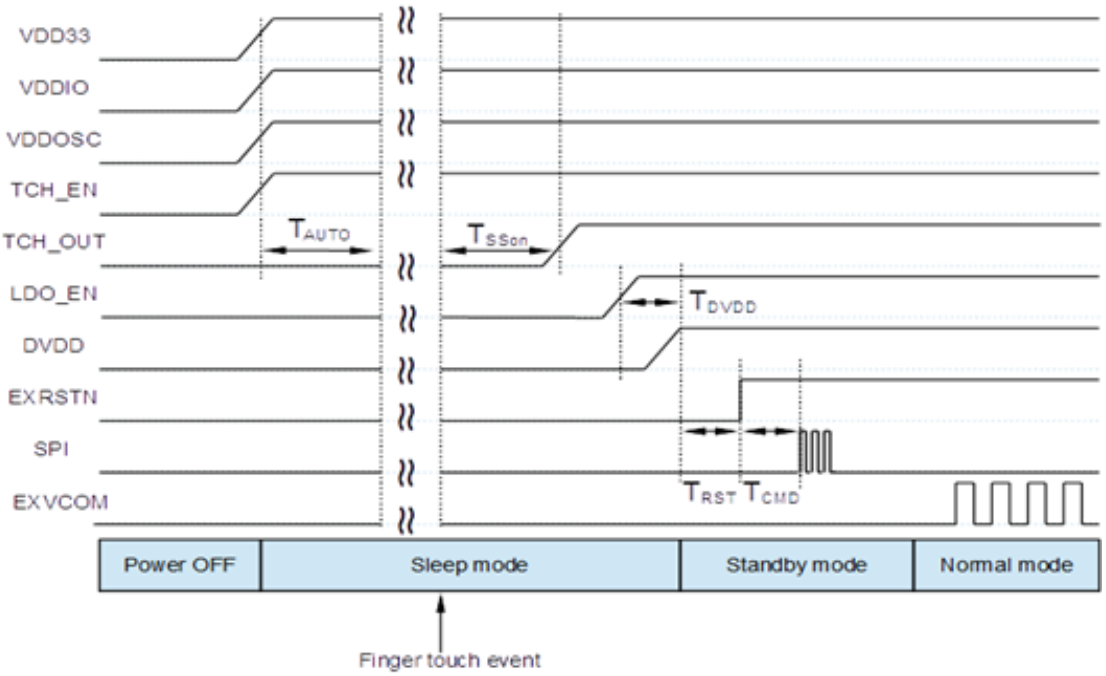
3. Connect Pin Define

Pin Number	Pin Name	Type	Pin Description
1	TCH_OUT	Output	Internal touch function output
2	SPI_MISO	Output	Data output pin for SPI interface
3	VDDIN	PWR	3.3V Power In(Min3.0V-Max3.6V)
4	RSTn	Input	System reset pin, Low active
5	SPI CLK	Input	Clock input pin for SPI interface
6	GND	GND	
7	SPI MOSI	Input	Data input pin for SPI interface
8	SPI CSn	Input	Chip select pin for SPI interface
9	ESD	ESD	Connect ESD pin to Ground.
10	LDO_EN	Input	Sensor internal power enable. (Default pull high) Connect to MCU GPIO is required

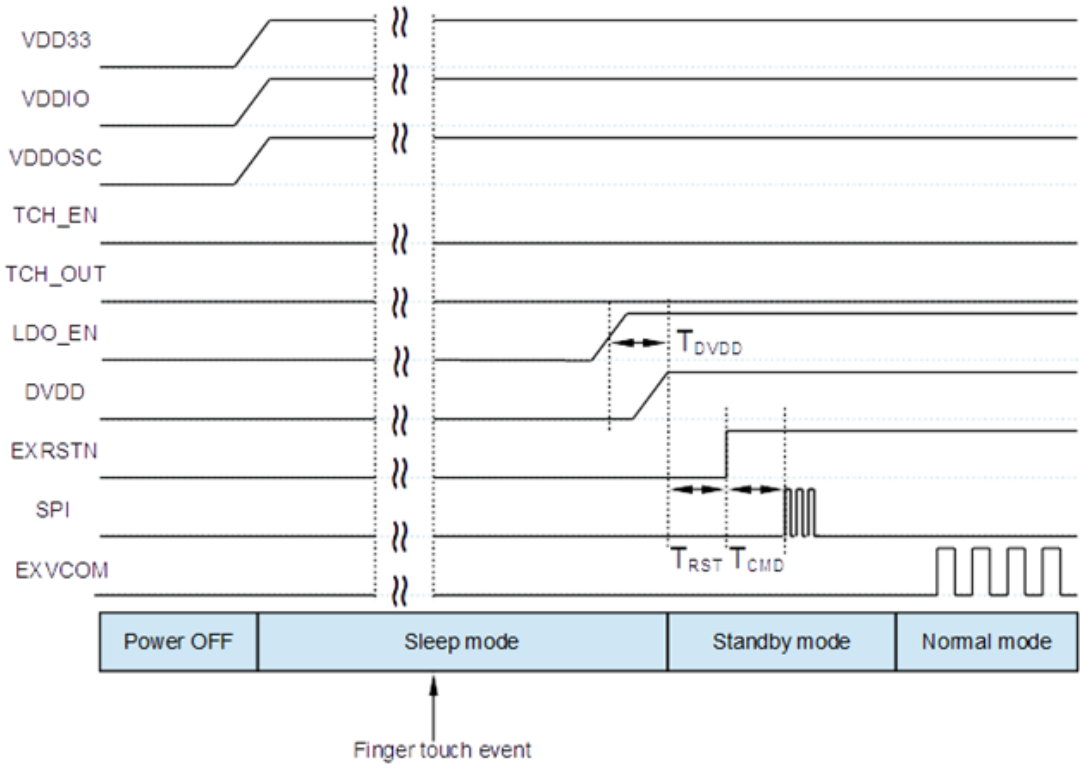


4. Power On Sequence

TCH_EN=1(Default)

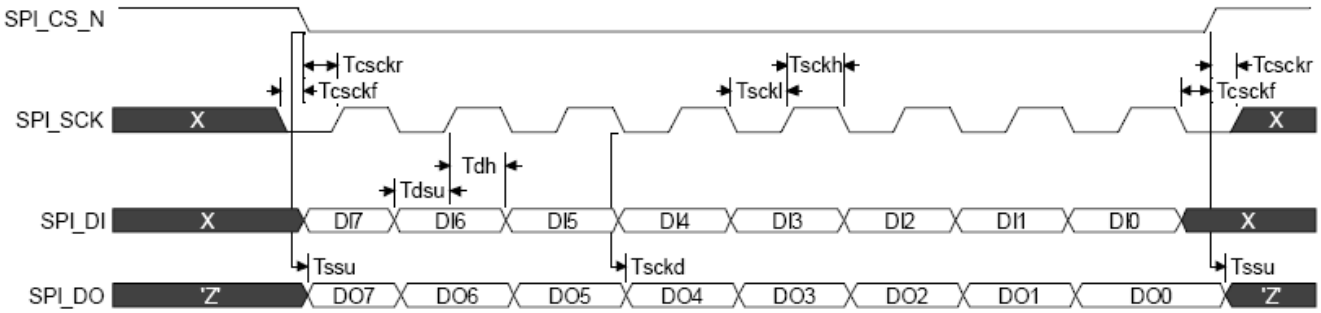


TCH_EN=0

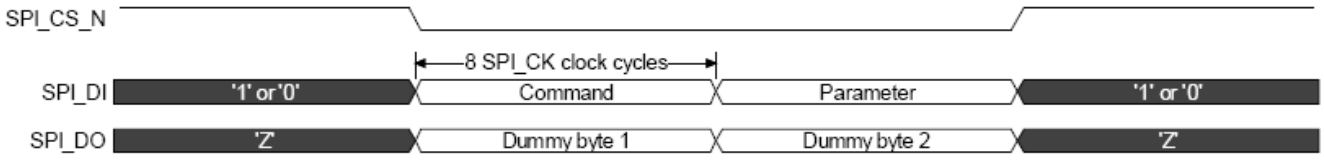


5. SPI Protocol

Symbol	Parameter	Min	Typ	Max	Units
Tauto	Touch sensor auto calibration time	300			ms

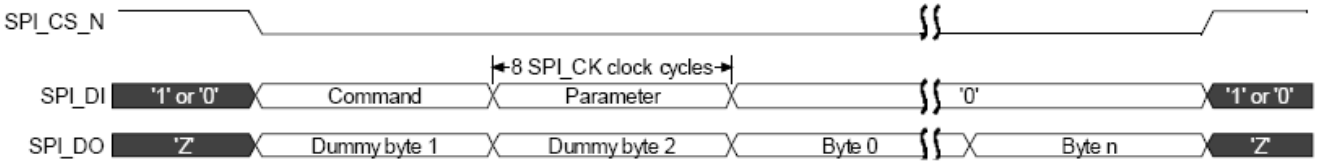


General SPI timing

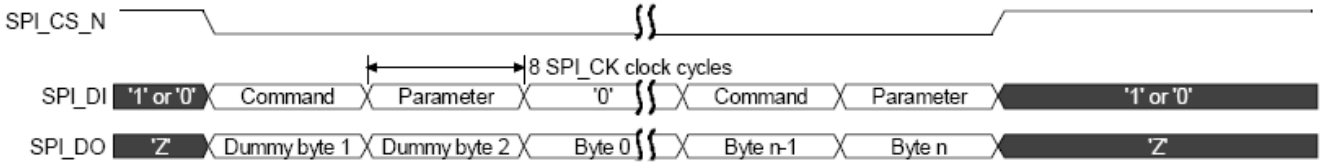


Instruction without return data

Instruction with return data



Terminating read by applying a new command



5.1 SPI Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
f_{CK}	Clock frequency		16	32	MHz
t_{RST}	Reset time	50			ns
t_{RD}	Rise time for digital inputs			2	ns
t_{FD}	Fall time for digital inputs			2	ns
f_{SPI_SCK}	Frequency for SPI clock.	0		f_{CK}	MHz
t_{SCKL}	Part of SPI_CK clock period, during which SPI_CK is low.	23			ns
t_{SCKH}	Part of SPI_CK clock period, during which SPI_CK is high.	23			ns

Symbol	Parameter	Min	Typ	Max	Units
t_{CSCKF}	Time from falling edge on SPI_CK to edge on SPI_CS_N	8			ns
t_{CSCKR}	Time from edge on SPI_CS_N to rising edge on SPI_CK	8			ns
t_{DSU}	Setup time for data before rising edge of SPI_CK	6			ns
t_{DH}	Hold time for data after rising edge of SPI_CK	6			ns
t_{SCKD}	Delay from falling clock to data available.	1		3	ns
t_{SSU}	Delay from SPI_CS_N low to SPI_DI mode change.	1		3	ns

5.2 SPI Commands

Send commands and set control registers through the SPI interface to control the operation. The SPI interface follows the SPI protocol with CPHA=0 and CPOL=0 as SPI mode 0. **The sensor only can support SPI mode 0 operation.**

These 7 command codes program the chip:

Command Code	Name	Function	Read/Write
0x01	RDATA	read pixel data	R
0x02	START	start scan	W
0x03	STATUS	read status	R
0x04	BR256	start 256 bytes burst	W
0x05	TCON	Read timing	R
0x06	BR032	start 32 bytes burst	W
0xC0	SRST	software reset	W
0x20+N	RREAD	read register	R
0x40+N	RWRITE	write register	W

For the register read and write commands, the number N is the register address. The effective N is in the range of 0x00 to 0x1F.

5.3 SPI Command Detail

Code 01 / RDATA command (read only)

- This command pumps image data from FIFO and sends it to the host.

Code 02 / START command (write only)

- This command starts the fingerprint image scan.

Code 03 / status read command (read only)

- This command sends the 8-bit internal status flags to the host.
- The status flags are defined as below

Bit	Function
0	Not defined, default always “0”
1	Not defined, default always “0”
2	Not defined, default always “0”
3	Not defined
4	Data FIFO is empty
5	Data FIFO is “half full”
6	Data FIFO is full
7	Image scan active

Code 05 / TCON read command (read only)

- This command sends the 8-bit internal status flags to the host.
- The status flags are defined as below

Bit	Function

Bit	Function
0	GSE256 decode timing
1	GSE256 decode timing
2	GSE256 decode timing
3	Not defined, default always “0”
4	Glass control timing
5	Glass control timing
6	Glass control timing
7	Glass control timing

Code 0xC0 / SRST command (write only)

- This command generates a software reset to the system. Its effect is the same as a hardware reset except that the register content is left unchanged.

Code 0x2N / register read command

- This command starts reading the register at address N.
- At least two bytes need to be written, the first byte is the command code, and the second (dummy) byte is for the register content.
- Subsequent register read commands can be cascaded in one command sequence.

Code 0x4N / register write command

- This command starts writing registers starting at address N.
- The first byte is the command code, followed by subsequent bytes that are written to registers starting at the specified starting address N.

All command code as the first byte in a command sequence returns the state byte (which can be explicitly read by the 03 command).

5.4 SPI Command Protocol

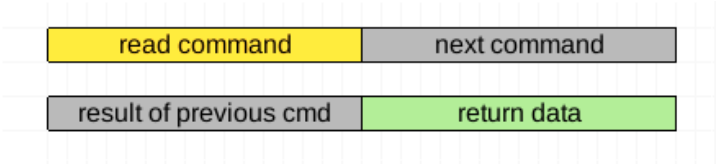
Command and data are exchanged through the SPI MISO and MOSI wires. Each byte of data sent through the MOSI port brings back a received byte through the MISO port.

Commands can be cascaded one after another. The term “SPI command sequence” in the following context is defined as a sequence of command code and data bytes exchange within one active SPISEL strobe.

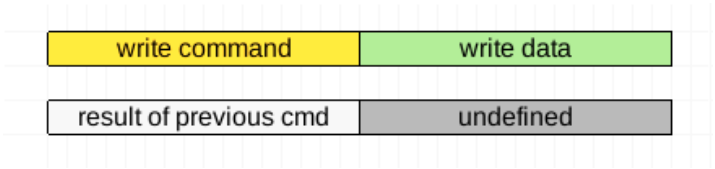
A command code may or may not have associated data. The “start scan” and “software reset” commands don’t have associated data, and take effect immediately after the command code is sent.

For read/write data commands, the second byte will be the beginning of the data byte or bytes, as illustrated below:

- Read command



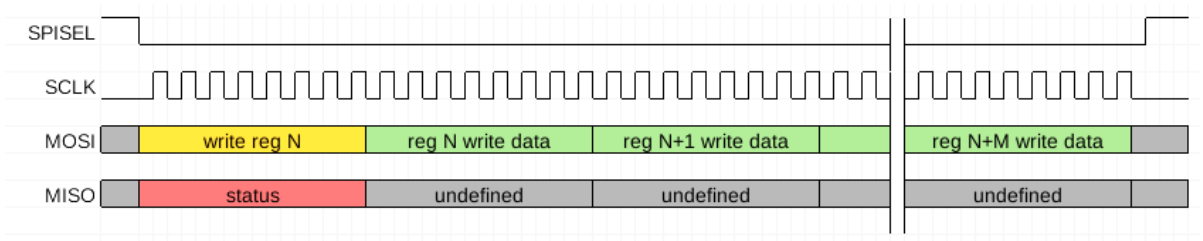
- Write command



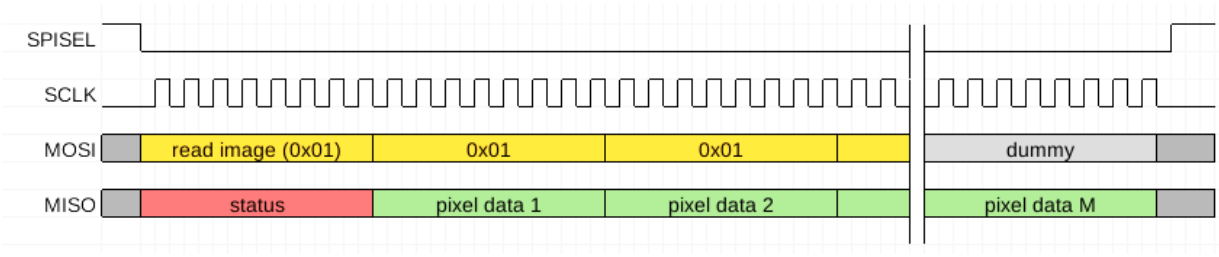
Writing and reading a series of register content may look different. For writing to consecutive registers, an internal address counter is incremented automatically after each byte written. This design eliminates the need to repeat sending the 0x40+N command for each byte. So the sequence of read/write commands may look like the following:

- Read sequence (the last command byte is a dummy command)

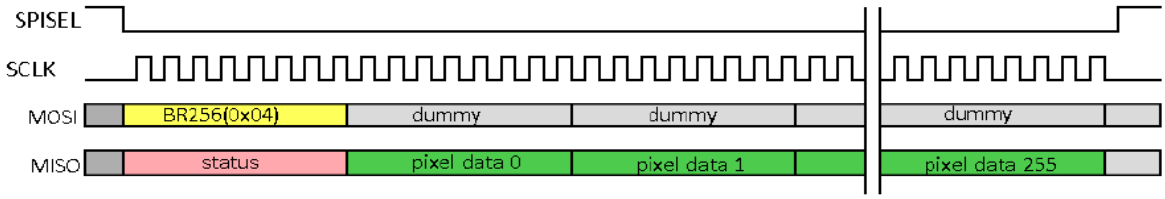
- Write sequence



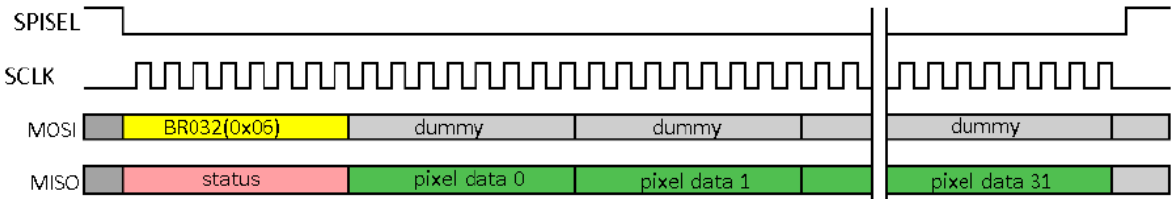
- Read image sequence



- Read image in burst 256 mode

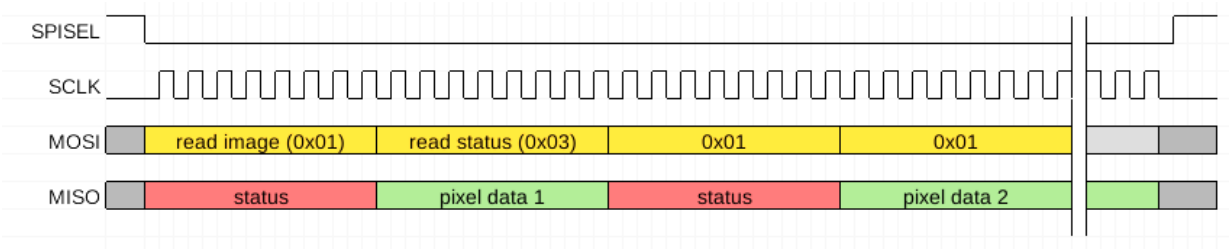


- Read image in burst 32 mode



In fact, except for the write register command (which writes a sequence of register content), commands can be mixed in a single sequence like the following:

- Mixed mode of read image and status sequence



6. Sensor Register

6.1 Register Table

N	Address	Name	Function	RW	Default Value	7	6	5	4	3	2	1	0
0	0x00	ID_H	high byte of ID	RO	0xF1	ID_H							
1	0x01	ID_L	low byte of ID	RO	0x31	ID_L							
2	0x02	AFE_CTL	afe control	RW	0x00	afe_cap_sel		i_afe_buf_sel		i_pre_amp_sel		afe_cap_sel_1	
3	0x03	ADC_CTL	adc control	RW	0x53	adc_vrb		adc_vref		i_adc_ctrl			
4	0x04	VLDO_TRM	vldo_trm	RW	0x24	dither_en	v2p4_en	v1p8_trm			v2p4_trm		
5	0x05	VR_TRM	vr_trm	RW	0x8C	trim_dac_dly			trim_de_meda		vr_trm		
6	0x06	QP_TRM	qp_trm	RW	0x84	trim_i_bias					qp_trm		
7	0x07	CALIB_OFFS	offset calibrating for 32 channels	WO	0x00	fw writes offsets for calibration							
8	0x08	CLOCK_CYCLE	operation clock control	RW	0xA0	op_clock_cycle		dec_clk_sel		invert_gls_rst	gpio_sel		
9	0x09	SEL_SF_NUM / PROCH_WIDTH	SUB_FRAME (H_SEL max) count / LAST_UNIT to next frame	RW	0x85	proch_width			sub_frame_num (int_hd_num[12:8])				
10	0x0A	BIST_STATUS	Bist status and error message	RO		bist_status (index:0~16)							
11	0x0B	RST_DELAY	RST delay time from INT_VD	RW	0x2D	int_vd_rst_width			int_hd_rst_width			rst_delay	
12	0x0C	RST_WIDTH	RST pulse width	RW	0x1C						rst_width		
13	0x0D	INT_HD_DELAY	INT_HD delay time from RST fall ed	RW	0x19	detctl_sel	bypass_dec	adj_dec_offset	invert_dout	intpo_first_line		int_hd_delay	
14	0x0E	rg_rsv_0	reserved byte 0	RO	hidden	KEY_H (hidden)							
15	0x0F	rg_rsv_1	reserved byte 1	RO	hidden	KEY_L (hidden)							
16	0x10	rg_dig_rsv	digital reserved byte	RW	0x00								
17	0x11	DIG_TEST	option of test	RW	0x00	test_adc		test_adc_sel					
18	0x12	INT_HD_WIDTH	INT_HD delay time from EXVCOM	RW	0x8A	hw_gated_dec	fw_gated_dec	int_hd_width					
19	0x13	DEC_OFFS	offset after GSE decoder	RW	0x00	after_dec_offset							
20	0x14	EXVCOM_DELA	EXVCOM delay time from INT_HD	RW	0x11		dec_gain_sel			calib_en	exvcom_delay		
21	0x15	EXVCOM_WIDTH	EXVCOM pulse width	RW	0x13					exvcom_width			
22	0x16	EXVCOM_NUM	EXVCOM pulse number	RW	0x04					pseudo_exv	exvcom_num		
23	0x17	EXVCOM_RST	EXVCOM pulse number/delay in RS	RW	0x69	avg_div_sel			exvcom_pulse_rst		exvcom_delay_rst		
24	0x18	OSC	oscillator	RW	0xE0	afe_rst_en	osc_en	tosc					
25	0x19	ANA_TEST	analog tester	RW	0x00								
26	0x1A	CQP_OFFS	dc offset of charge_pump	RW	0x81	cqp_dc_offset						i_buf_ctrl	
27	0x1B	LSF_TDAC	linear shift tdac	RW	0x00								
28	0x1C	rg_otp_addr_bite	OTP address & bit enable	RW	0x00	otp_addr					otp_bit		
29	0x1D	rg_otp_ctrl	OTP write control	RW	0x30			touch_ctl		otp_wpe (no use)	otp_prg	otp_rst	otp_ceb
30	0x1E	rd_otp_data	OTP read data	RO		otp_rdat							
31	0x1F	PAGE	page selection	RW	0x00	chip_en	vr_en	page_sel		analog_en	touch_rst	vsp_en	vsn_en

6.2 Register Setting For General Parameters

OP_CLOCK_CYCLE[1:0], It defines the period of clock.

OP_CLOCK_CY	Period of clock, T	Comments
0h	0.25us	
1h	0.5us	
2h	1.0us	Default
3h	2.0us	

V1P8_TRM[2:0], It defines the trimming value of V1P8 output.

V1P8_TRM	LDO output power for logic	Comments
0h	V1P8 - 0.20V	
1h	V1P8 - 0.15V	
2h	V1P8 - 0.10V	
3h	V1P8 - 0.05V	
4h	V1P8	Default
5h	V1P8 + 0.05V	
6h	V1P8 + 0.10V	
7h	V1P8 + 0.15V	

V2P4_TRM[2:0], It defines the trimming value of V2P4 output.

V2P4_TRM	LDO output power for logic	Comments
0h	V2P4 - 0.20V	
1h	V2P4 - 0.15V	
2h	V2P4 - 0.10V	

3h	V2P4 - 0.05V	
4h	V2P4	Default
5h	V2P4 + 0.05V	
6h	V2P4 + 0.10V	
7h	V2P4 + 0.15V	

VR_TRM[2:0], It defines the trimming value of VR1 output.

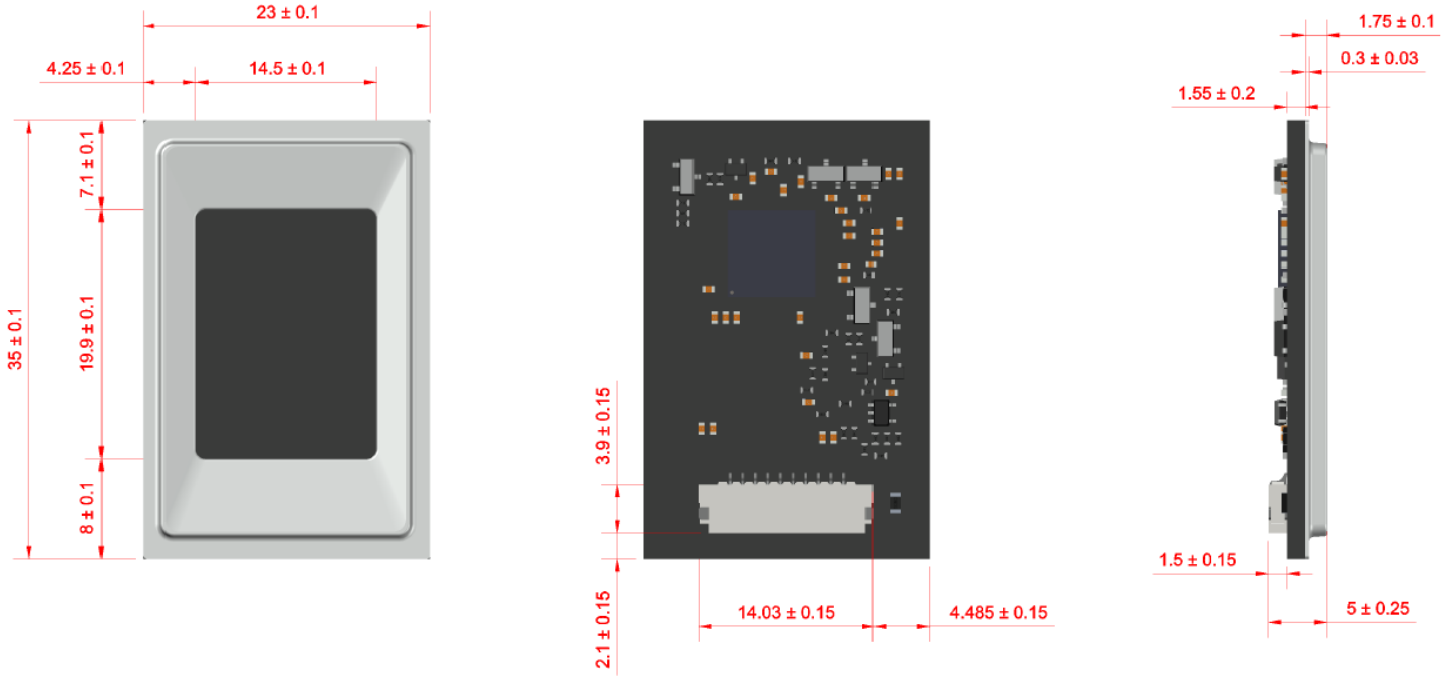
VR1_TRM	LDO output power for logic	Comments
0h	VR1-0.08V	
1h	VR1-0.06V	
2h	VR1-0.04V	
3h	VR1-0.02V	
4h	VR1	Default
5h	VR1+0.02V	
6h	VR1+0.04V	
7h	VR1+0.06V	

QP_TRM[2:0], It defines the trimming value of VP50 and VN50.

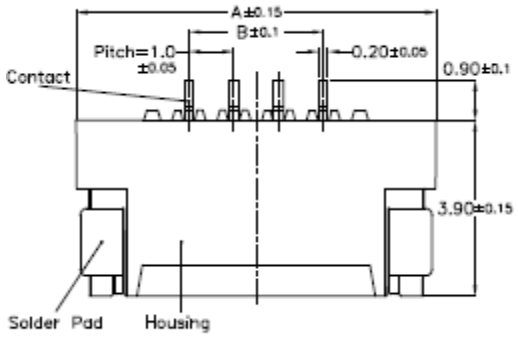
QP_TRM	Positive power	Negative power	Comments
0h	VP50 - 0.4V	VN50 + 0.4V	
1h	VP50 - 0.3V	VN50 + 0.3V	
2h	VP50 - 0.2V	VN50 + 0.2V	
3h	VP50 - 0.1V	VN50 + 0.1V	
4h	VP50	VN50	Default

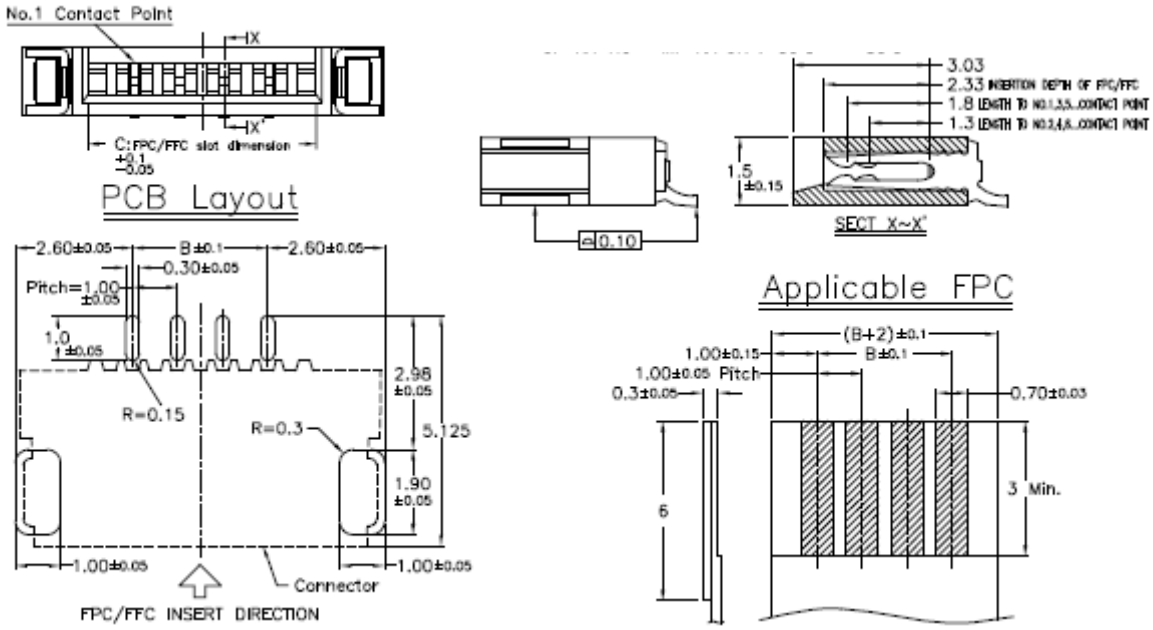
5h	VP50 + 0.1V	VN50 - 0.1V	
6h	VP50 + 0.2V	VN50 - 0.2V	
7h	VP50 + 0.3V	VN50 - 0.3V	

7. HF302GD Module 2D Drawing



8 Connector 2D Drawing





Revision History

Version	Date	Changes	Approved	Checked	Author
V0.4	**3/25**		Angus	Yehsuam	Sam